PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-122532
(43)Date of publication of application : 30.04.1999

(51)Int.Cl. H04N 5/335
H01L 27/146

(21)Application number : 09-261208
(22)Date of filing : 26.09.1997

(71)Applicant : SONY CORP
(72)Inventor : YONEMOTO KAZUYA
SUZUKI RYOJI

(30)Priority

Priority number :	09 54356	Priority date :	10.03.1997	Priority country :	JP
	09220265		15.08.1997		JP

(54) SOLID-STATE IMAGE PICKUP ELEMENT AND ITS DRIVE METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide the amplifier type solid-state image pickup element in which not only fixed pattern noise due to dispersion in characteristics for each unit pixel but also fixed pattern noise in a longitudinal stripe form is suppressed and to provide its drive method.

SOLUTION: In the amplifier type solid-state image pickup element comprising unit pixels 16 each consisting of a photo diode 11, an FD read MOS transistor(TR) 12, an FD amplifier MOS TR 13, an FD reset MOS TR 14 and a vertical selection MOS TR 15 and arranged in a matrix, a horizontal reset pulse ϕHRm outputted from a horizontal scanning circuit 24 is fed to a gate electrode of the FD reset MOS TR 14 and provides a one pixel signal to reset an FD of each pixel 16.

LEGAL STATUS

[Date of request for examination] 27.04.2004

[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3911788
[Date of registration]	09.02.2007
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

CLAIMS

[Claim(s)]

[Claim 1] The amplifier which has the are recording section in which the signal charge to which the unit pixel arranged in the shape of a matrix is transmitted from an optoelectric transducer and said optoelectric transducer is accumulated, and changes the signal charge of the are recording section concerned into an electrical signal, The solid state image sensor which is a solid state image sensor which comes to provide the selecting switch which outputs the pixel signal from said amplifier to a perpendicular signal line alternatively, and is characterized by having the reset circuit which resets the are recording section of each amplifier whenever it outputs a pixel signal in each of a unit pixel.

[Claim 2] Said reset circuit is a solid state image sensor according to claim 1 characterized by being a horizontal scanning circuit for making train selection of each of a unit pixel.

[Claim 3] Said reset circuit is a solid state image sensor according to claim 1 characterized by performing a reset action just before reading a pixel signal.

[Claim 4] The solid state image sensor according to claim 1 characterized by having the level selecting switch which outputs in common the signal before reset by said reset circuit drawn by said

perpendicular signal line, and the signal after reset between said perpendicular signal lines and level signal lines.
[Claim 5] The solid state image sensor according to claim 4 characterized by having the difference circuit which takes each difference of the signal before the reset outputted to said level signal line by said level selecting switch, and the signal after reset.
[Claim 6] Said difference circuit is a solid state image sensor according to claim 5 characterized by being a correlation duplex sampling circuit.
[Claim 7] Said optoelectric transducer is a solid state image sensor according to claim 1 characterized by consisting of an embedding photodiode.
[Claim 8] It is the solid state image sensor according to claim 1 which has a vertical-scanning circuit for making line selection of each of a unit pixel, and is characterized by the ability to set the timing relationship of two kinds of vertical-scanning pulses as arbitration while said vertical-scanning circuit gives two kinds of vertical-scanning pulses, a perpendicular selection scan pulse and a perpendicular read-out scan pulse, to a unit pixel through a separate signal line.
[Claim 9] Said horizontal scanning circuit is a solid state image sensor according to claim 2 which carries out the sequential output of the read-out scan pulse for reading a signal charge from said optoelectric transducer to said are recording section, and is characterized by performing the reset action of the are recording section of each unit pixel by the read-out scan pulse in the read-out timing in front of 1 train.
[Claim 10] The read-out gate section which reads a signal charge from said optoelectric transducer to said are recording section is a solid state image sensor according to claim 1 characterized by serving as overflow actuation of the superfluous signal charge of said optoelectric transducer.
[Claim 11] The solid state image sensor according to claim 10 characterized by setting the potential of said read-out gate section as potential higher than the potential of the component isolation region of said optoelectric transducer when said optoelectric transducer accumulates an electron as a signal charge.
[Claim 12] The solid state image sensor according to claim 10 characterized by setting the potential of the reset gate section which resets said are recording section when said optoelectric transducer accumulates an electron as a signal charge as potential higher than the

potential of said read-out gate section.
[Claim 13] The amplifier which has the are recording section in which the signal charge to which the unit pixel arranged in the shape of a matrix is transmitted from an optoelectric transducer and said optoelectric transducer is accumulated, and changes the signal charge of the are recording section concerned into an electrical signal, In the solid state image sensor which comes to provide the selecting switch which outputs the pixel signal from said amplifier to a perpendicular signal line alternatively Whenever it outputs a pixel signal in each of a unit pixel, the are recording section of each amplifier is reset. The drive approach of the solid state image sensor characterized by drawing the signal before reset, and the signal after reset from each of a unit pixel, and transmitting via a common transmission line, and taking each difference of the signal before reset, and the signal after reset after an appropriate time.
[Claim 14] The drive approach of the solid state image sensor according to claim 13 characterized by carrying out just before reading a pixel signal for the reset action of the are recording section of each amplifier in each of a unit pixel.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to a magnification mold solid state image sensor and its drive approaches, such as MOS mold image sensors with which it comes to arrange a unit pixel with a magnification function in the shape of a matrix, about a solid state image sensor and its drive approach.
[0002]
[Description of the Prior Art] Conventionally, the thing of a configuration of being shown in drawing 12 is known as this kind of a magnification mold solid state image sensor. Namely, it sets to drawing 12 . By a photodiode 101, FD (FloatingDiffusion) read-out MOS transistor 102, FD amplifier MOS transistor 103, FD reset MOS transistor 104, and perpendicular selection MOS transistor 105 The unit pixel 106 is constituted. The gate electrode of FD read-out MOS transistor 102 on the perpendicular read-out line 107 The gate electrode of perpendicular

selection MOS transistor 105 is connected to the perpendicular selection line 109, and the source electrode of perpendicular selection MOS transistor 105 is connected to the perpendicular signal line 110 for the gate electrode of FD reset MOS transistor 104 at the perpendicular reset line 108, respectively.

[0003] Moreover, level selection MOS transistor 112 is connected between the end of the perpendicular signal line 110, and the level signal line 111. And horizontal scanning pulse phiHm outputted from the horizontal scanning circuit 114 which actuation of a pixel is controlled by three kinds of vertical-scanning pulse phiVSn(s) outputted from the vertical-scanning circuit 113 which makes line selection, phiVTn, and phiVR for every line, and makes train selection A pixel signal is outputted to the level signal line 111 through level selection MOS transistor 112 controlled. In that case, the signal charge accumulated in the photodiode 101 by photo electric conversion is changed into the signal current by FD amplifier MOS transistor 103, and is drawn as an output signal of an image sensor.

[0004]

[Problem(s) to be Solved by the Invention] However, in the conventional magnification mold solid state image sensor of the above-mentioned configuration, the variation for every pixel of the property of FD amplifier MOS transistor 103, especially the Vth (threshold) variation of an MOS transistor will ride on the active element and the Lord who constitute each pixel as it is at the output signal of an image sensor. Since it has the value of immobilization for every pixel, the variation in this property is a fixed pattern noise (FPN;Fixed Patern Noise) on a screen. It appears by carrying out. Only in the part which needs to remove the noise component which establishes the noise rejection circuit which used a frame memory and the Rhine memory in the exterior of a device, and originates in the variation in the property of a pixel, therefore makes a noise rejection circuit external as a camera system, a scale will become large in order to oppress this fixed pattern noise.

[0005] On the other hand, the thing of a configuration of being shown in drawing 13 can be considered as a magnification mold solid state image sensor which enabled it to oppress a fixed pattern noise inside a device. in this magnification mold solid state image sensor , although the configuration of the unit pixel 106 be the same as drawing 12 , the water Hiraide force circuit 115 for oppress the fixed pattern noise resulting from the variation in the property of each pixel 106 be form , and it be different in that it be made to perform processing which take the difference of the signal before and behind read-out of a pixel 106

(before or after reset) in this water Hiraide force circuit 115 .
[0006] In drawing 13 , load MOS transistor 116 which works as a load of source follower actuation of FD amplifier MOS transistor 103 is connected between the perpendicular signal line 110 and the gland. Moreover, the main electrode of one way each of signal switch MOS transistor 117,117' of a pair is connected to the perpendicular signal line 110. Between the main electrode of each another side of signal switch MOS transistor 117,117' of this pair, and the gland, signal maintenance capacitor 118,118' of a pair is connected, respectively.
[0007] Moreover, between the main electrode of each another side of signal switch MOS transistor 117,117' of a pair, and level signal-line 111,111' of a pair, level selection MOS transistor 112,112' of a pair is connected, respectively. The noninverting (+) input edge of the differential amplifier 119 and the reversal(-) input edge are connected to level signal-line 111,111' of a pair, respectively.
[0008] In the magnification mold solid state image sensor of the above-mentioned configuration, each signal pixel reset before and after reset is held through signal switch MOS transistor 117,117' at signal maintenance capacitor 118,118', and is supplied to the differential amplifier 119 through level selection MOS transistor112,112' and level signal-line 111,111'. And in the differential amplifier 119, the fixed pattern noise resulting from the variation in the property for every unit pixel is removed by taking the difference of each signal pixel reset before and after reset.
[0009] however, in the magnification mold solid state image sensor of the above-mentioned configuration What [can be oppressed about the fixed pattern noise resulting from the variation in the property for every unit pixel] From resulting in the differential amplifier 119 through a separate signal path, each signal pixel reset before and after reset It will appear on a screen as a fixed pattern noise of the shape of a vertical reinforcement in which the variation in the property of signal switch MOS transistor 117,117' of a pair or level selection MOS transistor 112,112' of a pair has correlation perpendicularly. Therefore, also in this configuration, the amendment circuit for oppressing a vertical-reinforcement-like fixed pattern noise is [the exterior of a device] needed.
[0010] This invention is made in view of the above-mentioned technical problem, and the place made into the purpose is not only about the fixed pattern noise resulting from the variation in the property for every unit pixel but about a vertical-reinforcement-like fixed pattern noise to offer the magnification mold solid state image sensor which can be

oppressed inside a device, and its drive approach.
[0011]
[Means for Solving the Problem] The unit pixel arranged in the shape of a matrix the solid state image sensor by this invention An optoelectric transducer, The amplifier which has the are recording section which accumulates the signal charge transmitted from this optoelectric transducer, and changes the signal charge of the are recording section concerned into an electrical signal, The selecting switch which outputs the pixel signal from this amplifier to a perpendicular signal line alternatively is provided, and whenever it outputs a pixel signal in each of a unit pixel, it has composition equipped with the reset circuit which resets the are recording section of each amplifier.
[0012] In the solid state image sensor of the above-mentioned configuration, whenever the drive approach by this invention outputs a pixel signal in each of a unit pixel, it resets the are recording section of each amplifier, the signal before reset and the signal after reset are drawn from each of a unit pixel, and it transmits it via a common transmission line, and takes each difference of the signal before reset, and the signal after reset after an appropriate time.
[0013] In each of the unit pixel of the solid state image sensor of the above-mentioned configuration, the sequential output of the signal reset before and after reset is carried out for every pixel from each unit pixel by resetting the are recording section of each amplifier, whenever it outputs a pixel signal. Since the fixed pattern noise which originates in the variation in the property of a pixel at this time occurs as an offset component from the amplifier of each pixel, it can cancel a noise component by taking the difference of the signal reset before and after reset. Moreover, the noise component of the shape of a vertical reinforcement which has correlation perpendicularly is not theoretically generated with outputting the signal reset before and after reset to a level signal line via the same signal path from a perpendicular signal line, either.
[0014]
[Embodiment of the Invention] Hereafter, it explains to a detail, referring to a drawing about the gestalt of operation of this invention.
[0015] Drawing 1 is the block diagram showing the 1st operation gestalt of this invention. In drawing 1 , the unit pixel 16 is constituted by perpendicular selection MOS transistor 15 which are the photodiode 11 which is an optoelectric transducer, FD read-out MOS transistor 12, FD amplifier MOS transistor 13 which is an amplifier, FD reset MOS transistor 14, and a selection component, and two-dimensional

arrangement is carried out at the letter of a matrix. In addition, only the unit pixel 16 of eye a n line-m train is shown on the drawing for simplification.

[0016] this unit pixel 16 -- setting -- the gate electrode of FD read-out MOS transistor 12 -- the perpendicular read-out line 17 -- the gate electrode of perpendicular selection MOS transistor 15 is connected to the perpendicular selection line 19, and the source electrode of perpendicular selection MOS transistor 15 is connected to the perpendicular signal line 20 for the gate electrode of FD reset MOS transistor 14 at the level reset line 18, respectively. Moreover, level selection MOS transistor 22 is connected between the end of the perpendicular signal line 20, and the level signal line 21.

[0017] Moreover, the horizontal scanning circuit 24 for the vertical-scanning circuit 23 for line selection and train selection is formed. And perpendicular read-out scan pulse phiVTn outputted from the vertical-scanning circuit 23 To the perpendicular read-out line 17, it is perpendicular selection scan pulse phiVSn. It is impressed by the perpendicular selection line 19, respectively. Level reset pulse phiHRm outputted from the horizontal scanning circuit 24 To the level reset line 18, it is level selection scan pulse phiHSm. It is impressed by the gate electrode of level selection MOS transistor 22, respectively. That is, the horizontal scanning circuit 24 is level reset pulse phiHRm. Simplification of circuitry is attained by serving as the reset circuit to generate.

[0018] The correlation duplex sampling circuit (a CDS (Correlated Double Sampling) circuit is called hereafter) 25 where circuitry is easy is established in the outgoing end side of the level signal line 21 as a difference circuit which takes the difference of each signal pixel reset before and after reset. The concrete circuitry of this CDS circuit 25 and its circuit actuation are explained to a detail later. The outgoing end of the CDS circuit 25 is connected to the output terminal 26 of this image sensor.

[0019] Next, actuation of the magnification mold solid state image sensor concerning the 1st operation gestalt of the above-mentioned configuration is explained using the timing chart of drawing 2 .

[0020] First, the signal charge (electron) accumulated in the photodiode 11 by photo electric conversion When perpendicular read-out scan pulse phiVTn (phiVT1, --, phiVTn, phiVTn+1, --, phiVTN) is outputted from the vertical-scanning circuit 23 and FD read-out MOS transistor 12 flows in order for every pixel line It is transmitted to FD (the drain electrode of MOS transistor 12 = a photodiode 11 and main electrode of the

opposite side). A transfer of the signal charge from a photodiode 11 to FD is performed during a level blanking (H-BLK) period.

[0021] The potential of FD changes by a signal charge being transmitted to FD. The signal level of this FD is changed into the signal current by FD amplifier MOS transistor 13 by which the gate electrode was connected to FD. And if it enters at a level image period, perpendicular selection scan pulse phiVSn (phiVS1, --, phiVSn, phiVSn+1, --, phiVSN) will be outputted from the vertical-scanning circuit 23, and when perpendicular selection MOS transistor 15 will be in switch-on, the signal current will appear in the perpendicular signal line 20.

[0022] When level selection scan pulse phiHSm (phiHS1, --, phiHSm, phiHSm+1, --, phiHSM) will be outputted from the horizontal scanning circuit 24 during this level image period and level selection MOS transistor 22 will be in switch-on, the signal current which appeared in the perpendicular signal line 20 flows to the level signal line 21 through level selection MOS transistor 22, and is supplied to the CDS circuit 25 through this level signal line 21.

[0023] After that, immediately, to the same pixel which outputted the signal current, level reset pulse phiHRm (phiHR1, --, phiHRm, phiHRm+1, --, phiHRM) is outputted from the horizontal scanning circuit 24, and when FD reset MOS transistor 14 will be in switch-on, FD is reset. this level reset pulse phiHRm clear from the timing chart of drawing 2 -- as -- level selection scan pulse phiHSm between nascent states -- it is generated mostly in middle.

[0024] Therefore, level reset pulse phiHRm The signal charge of FD after disappearance, i.e., reset, is changed into the signal current by FD amplifier MOS transistor 13, and that signal current flows from perpendicular selection MOS transistor 15 to the level signal line 21 through the perpendicular signal line 20 and level selection MOS transistor 22, and is supplied to the CDS circuit 25 through this level signal line 21.

[0025] Thus, it is the horizontal scanning circuit 24 to level reset pulse phiHRm to one pixel 16 about a series of actuation called a signal output ->FD reset -> signal output. And level selection scan pulse phiHSm By outputting, it carries out one by one about the same pixel line. Moreover, the vertical-scanning circuit 23 to perpendicular read-out scan pulse phiVTn And perpendicular selection scan pulse phiVSn The signal current for one screen is outputted per pixel by outputting, changing the pixel line to choose and performing the same actuation.

[0026] If the pixel of eye a n line-m train is observed now, it is level selection scan pulse phiHSm. In the condition that start and the pixel

of eye m train is chosen, the signal current of the pixel reset before of FD and after reset will be outputted to the level signal line 21. That is, the signal current which is a pixel in the condition that the signal charge was accumulated, and the signal current which is a pixel in the condition that the signal charge was reset are outputted continuously, and is supplied to the CDS circuit 25. And in this CDS circuit 25, the variation component of the property of FD amplifier MOS transistor 13 is mainly removable by performing a correlation duplex sampling using the pixel signal reset before and after reset.

[0027] An example of the concrete circuitry of the CDS circuit 25 is shown in drawing 3 . The current potential conversion circuit 32 by which, as for this CDS circuit 25, the input edge was connected to the input terminal 31, The clamp capacitor 33 by which the end was connected to the outgoing end of this current potential conversion circuit 32, Clamp MOS transistor 34 by which one main electrode was connected to the other end of this clamp capacitor 33, Sample hold MOS transistor 35 by which one main electrode was connected to the other end of the clamp capacitor 33, The sample hold capacitor 36 connected between the main electrode of another side of this sample hold MOS transistor 35, and the gland, It consists of buffer amplifier 37 connected between the main electrode of another side of sample hold MOS transistor 35, and the output terminal 38.

[0028] In this CDS circuit 25, the current potential conversion circuit 32 consists of differential amplifier 39 which considers the signal current supplied through an input terminal 31 as a reversal (-) input, and considers predetermined bias voltage Vb as a noninverting (+) input, and a feedback resister 40 connected between the reversal input edge of this differential amplifier 39, and the outgoing end, and changes the signal current into a signal level. Clamp voltage Vcl is impressed to the main electrode of another side of clamp MOS transistor 34, and clamp pulse phiCL is impressed to the gate electrode, respectively. Moreover, sample hold pulse phiSH is impressed to the gate electrode of sample hold MOS transistor 35.

[0029] Next, circuit actuation of the CDS circuit 25 of the above-mentioned configuration is explained using the timing chart of drawing 4 .

[0030] Level selection scan pulse phiHSm If it starts, the signal current Isig before a pixel is reset will be inputted into an input terminal 31, and will be changed into a signal level Vsig by the current potential conversion circuit 32 with a reverse polarity. Clamp pulse phiCL stands according to the period when the signal level Vsig before

this pixel reset is outputted. Then, clamp MOS transistor 34 will be in switch-on, and clamps the clamp capacitor 33 to clamp voltage Vcl.
[0031] Then, level reset pulse phiHRm A pixel is reset by starting. And sample hold pulse phiSH stands according to the signal level Vsig after this pixel reset, sample hold is carried out to the sample hold capacitor 36, and a correlation duplex sampling is performed because sample hold MOS transistor 35 will be in switch-on. Thus, the variation component of the property of FD amplifier MOS transistor 13 is mainly removable by performing a correlation duplex sampling using the pixel signal reset before and after reset.
[0032] While being made to perform reset of FD of each pixel 16 whenever a 1-pixel signal is outputted as mentioned above By having been made to perform a correlation duplex sampling using the pixel signal reset before and after reset The fixed pattern noise of the shape of a vertical reinforcement resulting from the variation in the property of the switching device (level selection MOS transistor 22) connected to the fixed pattern noise and the perpendicular signal line 20 resulting from the variation in the property of a pixel can be oppressed.
[0033] That is, although it generates as an offset component from FD amplifier MOS transistor 13 of a pixel 16 about the fixed pattern noise resulting from the variation in the property of a pixel, it is removable theoretically by carrying out the correlation duplex sampling of the signal pixel reset before and after reset. Moreover, about the fixed pattern noise of the shape of a vertical reinforcement resulting from the variation in the property of the switching device connected to the perpendicular signal line 20, since the signal pixel reset before and after reset has composition which passes along the same signal path and it does not pass along separate switching devices (level selection MOS transistor etc.), this is not generated theoretically, either.
[0034] Drawing 5 is the block diagram showing the 2nd operation gestalt of this invention. They are the photodiode 51 whose unit pixel 58 is an optoelectric transducer in drawing 5 , the read-out gate section 52, and N+. It consists of FD53 which consists of a layer, FD amplifier MOS transistor 54, the FD reset gate section 55, perpendicular selection MOS transistor 56, and read-out control MOS transistor 57, and two-dimensional arrangement is carried out at the letter of a matrix. In addition, only the unit pixel 58 of eye a n line-m train is shown on the drawing for simplification.
[0035] It sets to this unit pixel 58, and, for a photodiode 51, a substrate front-face side is P+. It is the embedding mold covered with the layer. The read-out gate section 52 is located above the channel

between a photodiode 51 and FD53, and performs actuation which reads the signal charge by which photo electric conversion was carried out with the photodiode 51 to FD53. FD53 changes into a signal level the signal charge read from the photodiode 51. FD amplifier MOS transistor 54 changes and outputs the signal level changed by FD53 to the signal current.

[0036] And the gate electrode of FD reset gate section 55 is horizontal read-out line 59m-1 in front of 1 train. The gate electrode of perpendicular selection MOS transistor 56 is connected to the perpendicular selection line 60, the source electrode is connected to the perpendicular signal line 61, respectively, and, for the gate electrode of read-out control MOS transistor 57, the drain electrode is 59m of level read-out lines to the perpendicular read-out line 62. It connects, respectively. Moreover, level selection MOS transistor 64 is connected between the end of the perpendicular signal line 61, and the level signal line 63.

[0037] Moreover, the horizontal scanning circuit 66 for the vertical-scanning circuit 65 for line selection and train selection is formed. And perpendicular read-out scan pulse phiVTn outputted from the vertical-scanning circuit 65 To the perpendicular read-out line 62, it is perpendicular selection scan pulse phiVSn. Level read-out scan pulse phiHRm which is impressed to the perpendicular selection line 60, respectively, and is outputted from the horizontal scanning circuit 66 59m of level read-out lines Level selection scan pulse phiHSm It is impressed by the gate electrode of level selection MOS transistor 64, respectively.

[0038] In addition, the horizontal scanning circuit 66 is level read-out scan pulse phiHRm which serves as the reset circuit and is outputted from this horizontal scanning circuit 66. 59m of horizontal read-out lines While being given, it is horizontal read-out line 59m+1 of the following train. It is given as a reset pulse. At this time, it is horizontal read-out line 59m+1. It will function as a level reset line.

[0039] Here, wiring structure is explained. It considers as the three-layer wiring structure which forms the power-source line which serves the protection-from-light layer between the 2nd-layer wiring and pixels 58 both as the perpendicular signal line 61 which extends in the vertical direction of drawing, the perpendicular selection line 60 which extends the level read-out line 59 in the longitudinal direction of the 1st-layer wiring and drawing, and the perpendicular read-out line 62 as an example of wiring structure with the 3rd-layer wiring, respectively. It considers as the three-layer wiring structure which forms the power-

source line which serves the protection-from-light layer between the 2nd-layer wiring and pixels 58 both as the perpendicular selection line 60 which extends in the longitudinal direction of drawing, the perpendicular signal line 61 which extends the perpendicular read-out line 62 in the vertical direction of the 1st-layer wiring and drawing, and the level read-out line 59 as other examples with the 3rd-layer wiring, respectively.

[0040] The CDS circuit 67 where circuitry is easy is established in the outgoing end side of the level signal line 63 as a difference circuit which takes the difference of each signal the pixel reset back and before reset. The thing of the circuitry shown in drawing 3 used with the previous operation gestalt as this CDS circuit 67, for example is used. The outgoing end of the CDS circuit 67 is connected to the output terminal 68 of this image sensor.

[0041] Next, actuation of the magnification mold solid state image sensor concerning the 2nd operation gestalt of the above-mentioned configuration is explained using the timing chart of drawing 6 .

[0042] A certain light which carried out fixed period incidence embeds, photo electric conversion is carried out with a photodiode 51, and it is accumulated there as a signal charge. Here, before reading a signal charge from a photodiode 51 to FD53 (while the signal in front of 1 pixel is outputted), it is horizontal read-out scan pulse phiHRm-1 in front of [the horizontal scanning circuit 66 to] 1 train. It is outputted and is horizontal read-out line 59m-1. By minding and being impressed by the gate electrode of FD reset gate section 55, FD53 is beforehand reset by VDD level.

[0043] Just after that, it is level selection scan pulse phiHSm of eye m train from the horizontal scanning circuit 66. With being outputted, the signal output period of the pixel of eye a n line-m train comes. At this time, it is perpendicular selection scan pulse phiVSn. Since it is in the condition of "H" level and perpendicular selection MOS transistor 56 is in an ON state, in the first half in this signal output period, the signal in the condition that FD53 was reset is outputted to the perpendicular signal line 61 through FD amplifier MOS transistor 54 and perpendicular selection MOS transistor 56.

[0044] Moreover, at the second half in this signal output period, it is the horizontal scanning circuit 66 to level read-out scan pulse phiHRm. It is outputted and is 59m of level read-out lines. By minding, reading and being impressed by the drain electrode of control MOS transistor 57 In the gate electrode, it is perpendicular read-out scan pulse phiVTn. From being impressed MOS transistor 57 concerned will be in an ON state,

a signal charge is read from a photodiode 51 to FD53, and it is further outputted to the perpendicular signal line 61 through FD amplifier MOS transistor 54 and perpendicular selection MOS transistor 56.

[0045] Consequently, FD53 will take two potential conditions, the back before reading the signal charge of a pixel, during the signal output period of the pixel of eye a n line-m train it is going to output. And sequential supply of the signal current which amplifies those potential conditions by FD amplifier MOS transistor 54, and is acquired is carried out as the noise component equivalent to two potential conditions, the back before reading the signal charge of a pixel from the perpendicular signal line 61 to the CDS circuit 67 through level selection MOS transistor 64 and the level signal line 63, and a signal component.

[0046] Namely, perpendicular read-out scan pulse phiVTn outputted from the vertical-scanning circuit 65 in the n-th horizontal scanning period (1H) And perpendicular selection scan pulse phiVSn The pixel line of the n-th line is chosen by starting, respectively. Level selection scan pulse phiHSm and level read-out scan pulse phiHRm which are outputted from the horizontal scanning circuit 66 in the level image period except the level blanking period in this 1H period in order to scan the pixel line of the n-th line horizontally The sequential output of the signal current is carried out by starting, respectively.

[0047] The first half of a signal output period is the signal (noise component) level immediately after FD reset, and the items of a 1-pixel signal are set to the signal (signal component) level from which the second half read the pixel signal charge to FD53. In order to realize such actuation, it is level selection scan pulse phiHSm. And level read-out scan pulse phiHRm It is outputted to different timing. Namely, level selection scan pulse phiHSm If it attaches, it is set to "H" level in the 1-pixel whole period, and it is level read-out scan pulse phiHRm. If it attaches, it is the timing relationship set to "H" level only at the period when it is outputted in the second half of a 1-pixel period, i.e., a signal component.

[0048] Consequently, as point ** was carried out, FD53 of the pixel which it is going to output is beforehand reset in the period (level read-out scan pulse phiHRm- 1 period of "H" level) when the signal component is outputted from the pixel in front of one of them, and if it enters at the signal output period of the pixel, the signal in the condition that FD53 was reset, i.e., a noise component, will be outputted first.

[0049] And it is perpendicular read-out scan pulse phiVRn in the second half of a signal output period. It lets read-out control MOS transistor

57 which is in an ON state by being impressed by the gate electrode pass. Level read-out scan pulse phiHRm By reading and giving the gate electrode of the gate section 52 A signal charge is read from the embedding photodiode 51 to FD53, and by FD amplifier MOS transistor 54, the potential of FD53 changed by read-out of this signal charge is changed into the signal current, and is outputted as the signal of a pixel, i.e., a signal component.

[0050] Thus, the video signal which oppressed the fixed pattern noise resulting from the variation which FD amplifier MOS transistor 54 of each pixel has, especially Vth variation can be acquired by letting the CDS circuit 67 of the circuitry which shows the outputted signal current as an example to drawing 3 pass.

[0051] Here, the circuit actuation in the CDS circuit 67 of the circuitry shown in drawing 3 is explained using the timing chart of drawing 7 .

[0052] Level selection scan pulse phiHSm The signal current Isig of a noise component is inputted into an input terminal 31, and is changed into the signal level Vsig which the polarity reversed by the current potential conversion circuit 32 in the first half of the period in "H" level condition. Clamp pulse phiCL stands according to the period when the signal level Vsig of this noise component is outputted. Then, clamp MOS transistor 34 will be in switch-on, and initializes the potential of the node of the clamp capacitor 33 and sample hold MOS transistor 35 to clamp voltage Vcl.

[0053] Then, level selection scan pulse phiHSm Second half, i.e., level read-out, scan pulse phiHRm of the period in "H" level condition If the signal current Isig of a signal component is inputted into an input terminal 31 at the period in "H" level condition, the signal level Vsig which is equivalent to it from the current potential conversion circuit 32 will be given to input one end of the clamp capacitor 33. Thereby, only the electrical potential difference on which the potential by the side of the outgoing end of the clamp capacitor 33 is equivalent to the difference of the noise component and signal component changes on the basis of clamp voltage Vcl.

[0054] And sample hold pulse phiSH starts and the electrical potential difference which changes on the basis of clamp voltage Vcl is held at the sample hold capacitor 36 because this will be answered and sample hold MOS transistor 35 will be in switch-on. Thereby, Vth variation is removable to the variation component of the property which FD amplifier MOS transistor 54 of a pixel 58 has, and the Lord.

[0055] As mentioned above, in the 2nd operation gestalt, the fixed

pattern noise by the dark current can be effectively stopped by having used the embedding photodiode as a photodiode 51. That is, although the electron which becomes the dominant generating factor of the dark current from the level on the front face of a semi-conductor by thermal excitation is generated, it is P+ of the front face of a photodiode 51. The free charge which exists in a layer is only an electron hole, since an electron is in an exhaustion condition, surface level is filled in an electron hole and generating of the electron from surface level decreases remarkably. Therefore, the shot noise by dark current unevenness or the dark current is sharply mitigable.

[0056] Moreover, the fixed pattern noise by the Vth variation of FD amplifier MOS transistor 54 of each pixel can be oppressed by reading the signal charge from a photodiode 51 to FD53 to a pixel signal period, carrying out the sequential output of the signal before and behind read-out of a signal charge (a noise component and signal component), and carrying out the correlation duplex sampling of the output signal. And the signal before and behind read-out of a signal charge has composition which passes along the same signal path, and since it does not pass along a separate switching device (level selection MOS transistor), it can oppress also about the fixed pattern noise of the shape of a vertical reinforcement resulting from the variation in the property of the switching device connected to the perpendicular signal line 61.

[0057] Next, other examples of drive timing in the 2nd operation gestalt are explained. Drawing 8 is a timing chart which shows other examples of drive timing, and drawing 9 is a timing chart concerning circuit actuation of the CDS circuit 67 in the example of drive timing. At this example of drive timing, it is level read-out scan pulse phiHRm. After changing on "L" level, it is characterized by the point which read the signal component.

[0058] First, horizontal read-out scan pulse phiHRm-1 in front of [the horizontal scanning circuit 66 to] 1 train It is outputted and is horizontal read-out line 59m-1. FD53 is reset by VDD level by minding and being impressed by the gate electrode of FD reset gate section 55. Just after that, it is level selection scan pulse phiHSm of eye m train from the horizontal scanning circuit 66. With being outputted, the signal output period of the pixel of eye a n line-m train comes. At this time, the noise component amplified by FD amplifier MOS transistor 54 according to the level of reset FD53 is further outputted to the perpendicular signal line 61 through level selection MOS transistor 64 to the level signal line 63 through perpendicular selection MOS transistor 56.

[0059] Moreover, it is the horizontal scanning circuit 66 to level read-out scan pulse phiHRm during this signal output period. It is outputted and is 59m of level read-out lines. By minding, reading and being impressed by the drain electrode of control MOS transistor 57, MOS transistor 57 concerned will be in an ON state. And it lets this read-out control MOS transistor 57 pass, and is level read-out scan pulse phiHRm. By being impressed, since the read-out gate section 52 will be in an ON state, the signal charge accumulated in the photodiode 51 reads, and it is read to FD53 by the gate section 52.
[0060] Then, level read-out scan pulse phiHRm It disappears (it changes to "L" level). After it will read through read-out control MOS transistor 57 and the gate section 52 will be in an OFF state, The signal component amplified by FD amplifier MOS transistor 54 according to the signal charge read to FD53 is further outputted to the perpendicular signal line 61 through level selection MOS transistor 64 to the level signal line 63 through perpendicular selection MOS transistor 56.
[0061] Thus, the noise component and signal component equivalent to two potential conditions, the back before reading the signal charge of a pixel, are outputted to the level signal line 63, and the fixed pattern noise which originates in the variation which FD amplifier MOS transistor 54 of each pixel has, especially Vth variation by sequential supply being carried out further in the CDS circuit 67, and a correlation duplex sampling being performed is oppressed.
[0062] So that both the potentials that it is at the noise component's read-out and signal component's read-out time, read in this example of drive timing, and are especially impressed to the gate section 52 may become "L" level, i.e., same electric potential Level read-out scan pulse phiHRm Since it is considering as drive timing which reads a signal component after changing on "L" level, the fixed pattern noise resulting from the MOS transistor which constitutes the read-out gate section 52 can also be oppressed certainly.
[0063] Moreover, it sets to the solid state image sensor concerning this invention, and is perpendicular selection scan pulse phiVSn. And perpendicular read-out scan pulse phiVTn Electronic shutter actuation is also realizable by elaborating timing. Drawing 10 is perpendicular selection scan pulse phiVSn when performing electronic shutter actuation. And perpendicular read-out scan pulse phiVTn It is a timing chart.
[0064] When performing electronic shutter actuation, it is perpendicular read-out scan pulse phiVTn. The time of timing being normal operation is differed from. namely, -- the time amount which is equivalent to shutter

speed in front of the timing from which the pixel line of the n-th line is read — beforehand — perpendicular selection scan pulse phiVSn remaining as it is — perpendicular read-out scan pulse phiVTn only — make it stand — only read-out of the signal charge from a photodiode 51 to FD53 is performed.

[0065] The signal current amplified by FD amplifier MOS transistor 54 of the pixel of the n-th line supposing the pixel signal of the k-th line was outputted at this time is perpendicular selection scan pulse phiVSn. Since it does not stand, the pixel signal of the n-th line is mixed and is not outputted to the pixel signal of k lines. Consequently, the signal charge accumulated in the photodiode 51 is read at this time (reset), and are recording of a signal charge is again started from here, when the pixel line of the n-th line is read, it becomes, and the signal current corresponding to the signal charge accumulated by the time amount of shutter speed is outputted.

[0066] Moreover, the unnecessary signal charge beforehand read to FD53 in order to reset a photodiode 51 for the purpose of electronic shutter actuation is level read-out scan pulse phiHRm. FD53 is reset for every horizontal scanning, and is absorbed by the reset drain (N+ layer) connected to the power source VDD.

[0067] Drawing 11 is drawing having shown signs that overflow (anti blooming) actuation which inhibits the phenomenon of a blooming, like the read-out gate section 52 leaks and is crowded in the pixel which the signal charge (electron) which a superfluous light carried out [the signal charge] incidence to the photodiode 51, and carried out photo electric conversion to it adjoins could be performed. This drawing shows the potential diagram applied to FD reset gate section 55 from a photodiode 51 about 4 of an are recording condition (A), a read-out condition (B), FD reset condition (C), and an overflow condition (D) conditions.

[0068] Here, the signal charge generated superfluously overflows to FD53 through FD read-out gate section 52 by strong incident light by setting up more highly than 0V (potential of the component isolation region of a photodiode 51) potential phiROG of FD read-out gate section 52 in an are recording condition (A) (overflow actuation). The signal charge overflowed at this time is reset by FD reset action performed just before every horizontal scanning and a pixel signal are read to FD53, and can be prevented from having a bad influence on a video signal.

[0069] Furthermore, when a strong light which overflows to FD53 by overflow actuation carries out incidence By setting up more highly than potential phiROG of FD read-out gate section 52 in an are recording

condition (A) potential phiRG of FD reset gate section 55 in an are recording condition (A) Without the signal charge which overflowed with FDs53 flowing backwards to a photodiode 51, it is absorbed by the reset drain through FD reset gate section 55, and can avoid having a bad influence on a video signal.

[0070] Thus, it is perpendicular selection scan pulse phiVSn about a vertical-scanning pulse. And perpendicular read-out scan pulse phiVTn It also becomes possible by dividing into two lines and setting up the timing relationship suitably to perform electronic shutter actuation. And pixel size can be made small by having considered as the structure of also giving overflow actuation of a pixel signal besides read-out actuation to the read-out gate section 52.

[0071] In addition, in each above-mentioned operation gestalt, although the case where it applied to the magnification mold solid state image sensor of the configuration using FD amplifier (floating diffusion amplifier) as an amplifier which constitutes a unit pixel was explained, this invention is not limited to this and can be applied also like the magnification mold solid state image sensor of the configuration using [for example,] FG amplifier (floating-gate amplifier) as an amplifier.

[0072]

[Effect of the Invention] In the solid state image sensor with which it comes to arrange a unit pixel with a magnification function in the shape of a matrix according to this invention as explained above Since the sequential output of the signal reset before and after reset is carried out for every pixel from each unit pixel by having reset the are recording section of each amplifier whenever it outputs a pixel signal in each of a unit pixel Since a fixed pattern noise can be oppressed and the signal reset before and after reset can moreover be outputted to a level signal line via the same signal path from a perpendicular signal line by taking the difference of the signal reset before and after reset, Generating of a vertical-reinforcement-like fixed pattern noise can also be suppressed.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the 1st operation gestalt of this invention.

[Drawing 2] It is a timing chart for explanation of the 1st operation gestalt of operation.
[Drawing 3] It is the circuit diagram showing an example of the configuration of a CDS circuit.
[Drawing 4] It is a timing chart for explanation of the CDS circuit in the 1st operation gestalt of operation.
[Drawing 5] It is the block diagram showing the 2nd operation gestalt of this invention.
[Drawing 6] It is a timing chart for explanation of the 2nd operation gestalt of operation.
[Drawing 7] It is a timing chart for explanation of the CDS circuit in the 2nd operation gestalt of operation.
[Drawing 8] It is the timing chart which shows other examples of drive timing concerning the 2nd operation gestalt.
[Drawing 9] It is a timing chart for explanation of the CDS circuit in other examples of drive timing concerning the 2nd operation gestalt of operation.
[Drawing 10] It is the timing chart of the vertical-scanning pulse at the time of electronic shutter actuation.
[Drawing 11] It is a potential Fig. explaining anti blooming actuation.
[Drawing 12] It is the block diagram showing the conventional example.
[Drawing 13] It is a block diagram for explaining a technical problem.
[Description of Notations]
11 -- A photodiode, 12 -- FD read-out MOS transistor, 13 54 -- FD amplifier MOS transistor, 14 -- FD reset MOS transistor, 15 56 -- 16 A perpendicular selection MOS transistor, 58 -- Unit pixel, 17 62 -- A perpendicular read-out line, 18 -- 19 A level reset line, 60 -- Perpendicular selection line, 20 61 -- 21 A perpendicular signal line, 63 -- 22 A level signal line, 64 -- Level selection MOS transistor, 23 65 -- 24 A vertical-scanning circuit, 66 -- 25 A horizontal scanning circuit, 67 -- CDS (correlation duplex sampling) circuit, 51 [-- FD reset gate section, 59 / -- Level read-out line (level reset line)] -- An embedding photodiode, 52 -- The read-out gate section, 53 -- FD (floating diffusion), 55